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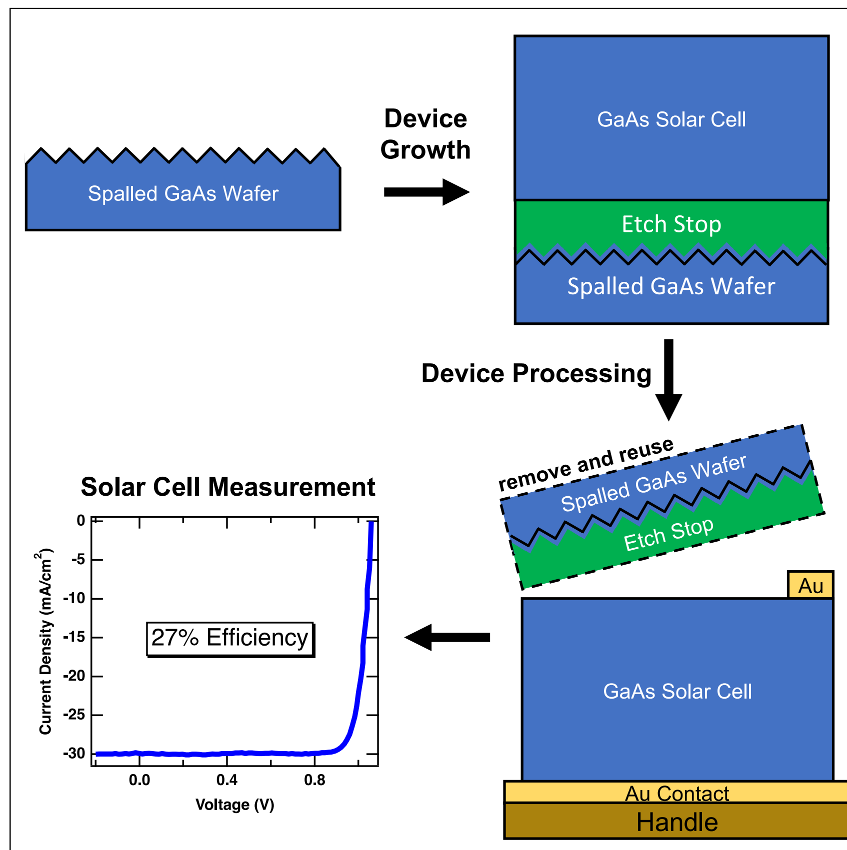
GaAs solar cells grown on acoustically spalled GaAs substrates with 27% efficiency



Acoustically spalled substrates offer the potential for cost reduction in high-efficiency III–V photovoltaics, but spalling can generate features on the substrate surface that may complicate epitaxial growth of subsequent devices. We grew GaAs solar cells on previously spalled surfaces and developed control over defects that stem from growth over surface features. Using this understanding, we demonstrated a GaAs solar cell with 27% efficiency on a previously spalled surface.

Kevin L. Schulte, Steve W. Johnston, Anna K. Braun, ..., Mariana I. Bertoni, Emily L. Warren, Myles A. Steiner

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Highlights

Acoustically spalled substrates offer the potential for substrate reuse

GaAs solar cells are grown on acoustically spalled GaAs substrates

Device defects resulting from spalled surfaces are characterized and mitigated

We show a GaAs solar cell with 27% efficiency on an acoustically spalled substrate

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GaAs solar cells grown on acoustically spalled GaAs substrates with 27% efficiency

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SUMMARY

Acoustic spalling presents a potentially low-cost reuse pathway for III–V epitaxial growth substrates via exfoliation of device layers with recovery and reuse of the substrate. However, surface features formed during spalling can reduce the performance of subsequently grown devices. We develop an understanding of how the surface morphology of acoustically spalled substrates affects GaAs solar cell performance and develop strategies to mitigate these impacts. We demonstrate that minor planarization of the surface by wet chemical etching and/or epitaxial growth, or the redesign of the device structure to thicken critical layers, prevents performance degradation. Using these strategies, we demonstrate a 0.25 cm^2 single-junction GaAs device with 26.9% $\pm$ 0.2% photovoltaic conversion efficiency under the AM1.5G spectrum grown on an acoustically spalled substrate. These results enable the growth of high-performance III–V devices on non-traditional substrates with the potential for significantly reduced device costs.

CONTEXT & SCALE

III–V solar cells offer the highest solar photovoltaic conversion efficiencies of any technology, but high manufacturing costs limit their use in terrestrial applications. Roughly one-third of the cost of a III–V solar cell comes from the single-crystalline substrate on which it is grown. Acoustic spalling is a new process that enables the rapid cleavage of III–V devices from their parent substrates, potentially enabling substrate reuse *if* high-efficiency devices can be grown on previously spalled substrates.

In this work, we study the vapor growth of GaAs solar cells on previously spalled GaAs substrates and develop an understanding of how the spalled surface affects subsequent device growth and performance. We develop a GaAs device grown on a previously spalled substrate with 27% efficiency, which compares favorably to GaAs efficiencies obtained on *any* III–V substrate. These results highlight the potential of acoustic spalling as a viable substrate reuse technology.

INTRODUCTION

III–V photovoltaics exhibit the highest photovoltaic conversion efficiencies of any material class,[1] but are generally regarded as a niche technology that is reserved for high-performance applications, such as space power, due to their high manufacturing cost.[2] Numerous emerging terrestrial applications,[3] such as thermal energy grid storage,[4] unmanned aerial vehicles,[5] portable power, and vehicle integrated photovoltaics,[6] would benefit from the application of III–Vs, but nearly perfect materials that are epitaxially synthesized on single-crystalline growth substrates are required to achieve the highest efficiencies. Current estimates suggest that III–V solar cells cost ~\$150/W, with epitaxial growth, substrates, and cell processing each accounting for roughly one-third of that total.[7]

One way to reduce the cost of growth substrates is to recover and reuse them. Epitaxial lift-off (ELO), a process in which the device is separated from the substrate by lateral selective etching of a buried sacrificial layer, is presently used by industry to recover growth substrates. However, this process uses large amounts of HF etchant, is relatively slow (on the order of 10 h for 150 mm wafers), and requires periodic chemical mechanical polishing (CMP) of the substrates to clear insoluble etch products that build up over time.[8] CMP is estimated to cost ~\$25 per cycle,[7] which sets a lower limit on the substrate cost even if a substrate could be reused an infinite number of times.[9]

Spalling of III–V epitaxial devices from their parent substrate is emerging as a promising method for cost-effective substrate recovery.[10] Spalling works via the

application of an external stressor layer, such as electroplated Ni, to the epilayer/substrate stack after growth, which controls the mechanical cleavage of the epilayer from the substrate at a depth prescribed by the stressor. The process is fast, with the cleavage taking only seconds, and potentially CMP free because a contamination-free surface is revealed from within the crystal with each spall. One challenge is that spalling of the (100) orientation of GaAs, which is the dominant substrate orientation for nearly all III–V device growth, traditionally results in the formation of facets with >5 μm peak-to-trough height due to propagation of the cleave along inclined {110} or {211} planes.[11,12] These large facets may necessitate the use of thick epitaxially grown protection layers or other significant planarization before device regrowth, adding cost.[9] Acoustic spalling, or sonic lift-off (SLO), is a spalling process under development that uses sound waves to control the propagation of the crack tip during the spall in order to suppress facet formation and improve surface flatness.[13] SLO was shown to reduce facet height in (100)-GaAs spalling,[14,15] which could make substrate reuse via spalling a viable commercial process by generating a surface requiring minimal re-preparation before subsequent device growth. This study seeks to understand the level of device performance enabled by the present level of roughness created by SLO and to develop strategies for achieving high photovoltaic efficiency on non-traditional substrates.

In this work, we study the growth of GaAs solar cell devices on acoustically spalled substrates with regions containing faceted surfaces. We identify the formation of efficiency-reducing, non-linear shunt defects in regions of non-flat epitaxial growth across spalling-related facets exceeding 2–3 μm peak-to-valley height. We show that these defects can be mitigated by modest planarization of the facets via wet etching and growth or by optimization of the device structure to thicken critical layers. We demonstrate devices grown on SLO surfaces with near-parity to devices grown on CMP-polished, "epitaxy-ready" substrates obtained directly from a wafer manufacturer, with conversion efficiency up to 26.9% ± 0.2% under the AM1.5G solar spectrum. We discuss further strategies to improve device performance.

RESULTS

First, we grew an upright device on an epi-ready substrate, a SLO substrate, and a SLO substrate etched in a 2:1:10 NH_4OH:H_2O_2:H_2O solution (see experimental procedures) for 3 min to determine the effect of the acoustically spalled surface on device performance. Note that the SLO devices were grown on previously spalled wafers, and all devices were left on the wafer. Figure 1A shows the device structure. Figures 1B and 1C show the external quantum efficiency (EQE) and light current density-voltage (*J-V*) curves for these devices, respectively. Note that the multiple *J-V* curves for each substrate type come from multiple devices fabricated from a single growth on each substrate type. The EQEs are nearly equal in terms of magnitude and shape for all three samples. This result suggests that the minority carrier diffusion length is high (multiple μm) in all samples and did not degrade significantly due to growth on the rougher spalled substrates.[16] There is a large variance in the light *J-V* performance, however. The open-circuit voltage (V_{OC}), or the voltage at which the light *J-V* curve crosses 0 mA/cm^2, for the control devices is ~1.03 V with little variance, typical of on-wafer front-junction GaAs cells.[17] The V_{OC}s for the devices grown on the SLO substrate are much lower, with a range of 0.49–0.68 V. A low V_{OC} indicates a high degree of carrier recombination, which usually indicates the presence of a defect. The devices grown on the wet-etched SLO substrates exhibit improved V_{OC} but with a wide variance in the range 0.72–1.01 V. The dark *J-V* curves in Figure 1D provide more insight into the device behavior. The control *J-V*s have the

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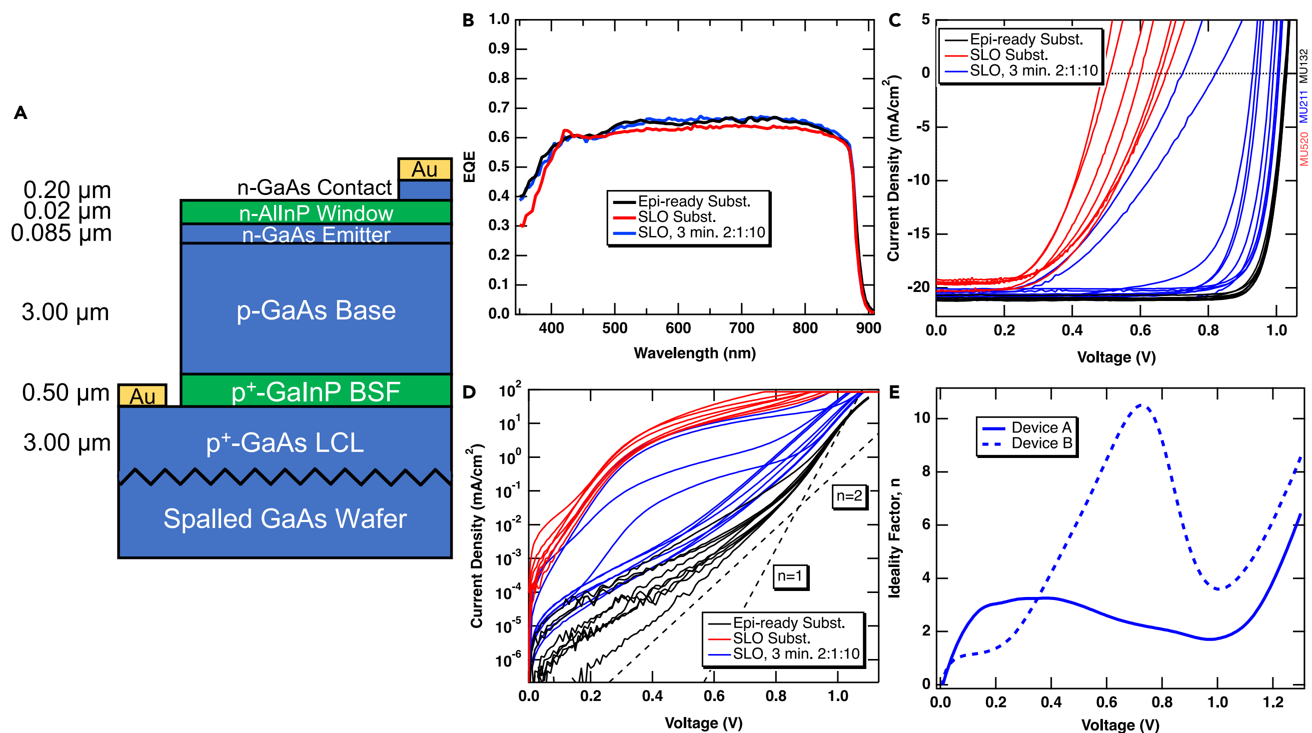

Figure 1. Impact of sonic lift-off surface on device performance

(A–D) (A) Upright device structure for a device grown on spalled SLO substrate. External quantum efficiency (B), light current density-voltage curves (C), and dark current density-voltage curves (D) for devices grown on epi-ready, SLO, and wet-etched SLO substrates. The broken lines in (D) indicate slope corresponding to diodes with ideality factor n = 1 and n = 2.

(E) Ideality-voltage curves for devices without (device A) and with (device B) non-linear shunting.

expected shape, with a diode ideality of n ~ 2 at low voltages that decreases and approaches n ~ 1 closer to V_{OC} as the limiting dark current shifts from Shockley-Read-Hall (SRH) recombination in the depletion region to radiative recombination in the quasi-neutral regions. All of the devices grown on the as-spalled SLO substrate exhibit regions of atypical ideality of n >> 2 and generally high dark current. The etched SLO substrate has some devices with *J-V*s that look similar to those grown on the control substrate and some with the n >> 2 behavior of the as-spalled devices. The n >> 2 behavior suggests the presence of a shunt, but its behavior is non-linear because the elevated ideality factor does not persist at low voltage.[18] An ideality-voltage (*n-V*) plot, which plots the local ideality, proportional to dV/dln(*J*), calculated at each voltage, highlights the effect of the non-linear shunt. Figure 1E shows *n-V* curves for a non-shunted (device A) and shunted (device B) device from the etched SLO sample. Device A device exhibits an ideality just above n = 2 at low voltage, then decreases with voltage toward n = 1, with a minimum at *V* ~ 1. The ideality increases sharply with voltage above this minimum due to the effect of series resistance. For device B, n ~ 1 from 0 to 0.2 V, but then increases sharply to a peak just above n ~ 10 at V = 0.73 V. n rapidly decreases above 0.73 V but increases again with voltage as series resistance dominates the *n-V* curve above 1 V. The clear peak in the *n-V* curve of device B provides a signature of the presence of the non-linear shunt. The question becomes what makes the performance of devices A and B so different despite being from the same growth?

We employed dark lock-in thermography (DLIT) to look for the source of the non-linear shunting. DLIT uses an infrared camera to identify regions of the solar cell device that

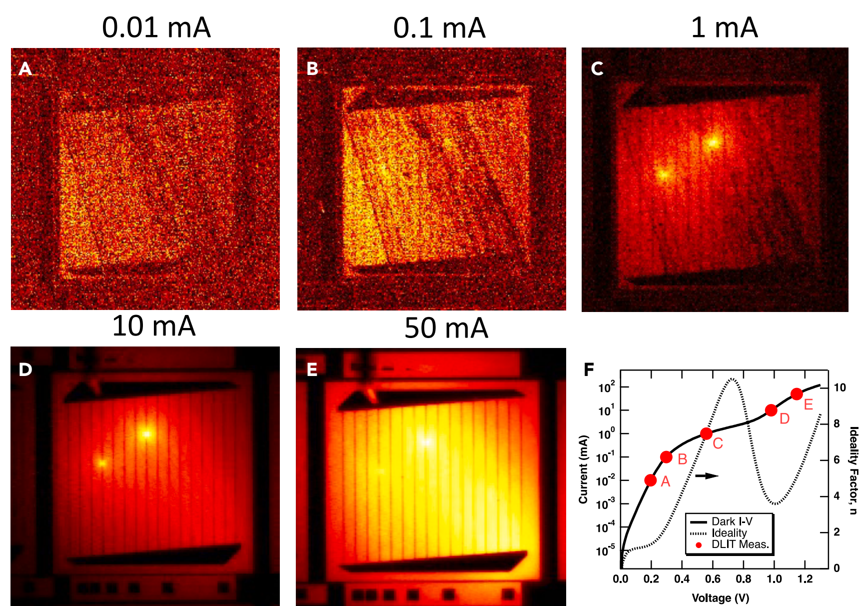

Figure 2. Dark lock-in thermography of a non-linearly shunted device

(A–E) Dark lock-in thermography images taken from device B of Figure 1E under varying current-voltage conditions.

(F) Dark *I-V* curve for this device, with *I-V* condition at which each image was acquired indicated by a red dot. The *n-V* curve is plotted on the mirror y axis.

heat up due to Joule heating where current is flowing. Figures 2A–2E show thermal images of device B of Figure 1E taken under varying current-voltage conditions. Figure 2F shows the dark current-voltage (*I-V*) and *n-V* curves for this device, with red dots indicating the position on the *I-V* curve at which each DLIT image was captured. At low current injection (panels A and B), we do not see evidence of shunting, and the device heating is low. We note that there are dark diagonal lines, which we attribute to emission that is not picked up by the camera due to the reflection of light by faceted areas related to the spall. In panel C, which is taken on the portion of the dark *I-V* curve where the ideality factor is approaching its peak (see panel F), we see two shunted regions that are significantly hotter than the surrounding device area appear in the image. The fact that these shunts did not appear at $V = 0$ confirms that they are not simple shunts (e.g., shorting of the front and rear contacts), but more complex, non-linear shunts. The image in panel D, which is taken after the peak in the *n-V* curve, shows that the shunted areas are still the hottest, but the rest of the area begins heating substantially, indicating that the main n-p diode is starting to turn on. The main diode continues heating as shown in panel E, although the shunts are still somewhat visible. We note that Joule heating due to series resistance at the contacts or in the lateral conduction layer (LCL) is likely contributing to heating in this last image due to its position on the second increasing part of the *n-V* curve.

We examined one of the shunts observed in the DLIT images more closely using Nomarski contrast optical microscopy and scanning electron microscopy (SEM) to resolve the structure of this defect. Figure 3A shows a composite of an optical microscopy image and a DLIT image of the larger defect observed in Figure 2D. We see that the heating occurs in a region where the grid line looks significantly rougher and possibly discontinuous over a portion of the sample containing larger facets. Looking at this area in plan-view SEM, in Figure 3B, we see that the gridline sank into a trench between two overgrown facets. We then used a focused ion beam

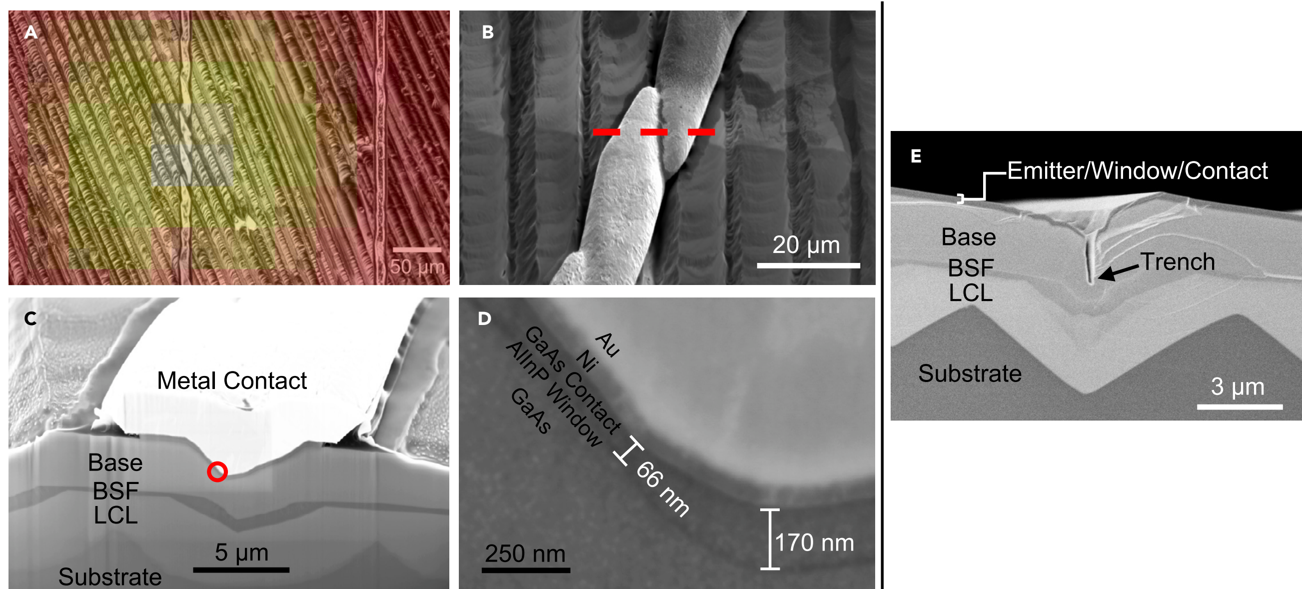

Figure 3. Structural analysis of a non-linear shunt defect

(A) Composite DLIT/Nomarski microscopy image of the larger shunt defect observed in Figure 2D.

(B) SEM image focused on the rough gridline observed in (A).

(C) Cross-sectional SEM image of the area under the gridline, roughly indicated by the dashed line in (B). This cross-section was obtained by removing some of the material using an SEM-FIB.

(D) Magnified image of the area in the red circle in (C) showing the thinner, upper layers of the device.

(E) Cross-sectional SEM image of a separate area of the device taken before processing where a trench in the epitaxial layers was observed.

(FIB) to mill a trench in this area, roughly indicated by the red broken line in Figure 3B, and expose the cross-section for SEM imaging, shown in Figure 3C. This image shows that the epitaxial device structure is disrupted by the underlying morphology of the substrate. There are facets with peak-to-valley heights of 2–3 μm in the substrate. The GaAs LCL planarizes over the substrate facets somewhat, but still leaves a significant trench in between them. The GaInP back surface field (BSF) planarized the trench further, but the GaAs base and emitter, AlInP window, and GaAs contact are significantly disrupted above the trench. The GaAs base varies from 2.8 μm (close to the nominal 3.0 μm) to 1.4 μm at its thickest and thinnest points, respectively. The electroplated metal contact gridline filled this trench during device processing. Figure 3D shows another cross-sectional SEM image focused closer on the thin layers above the base in the region indicated by the red circle in Figure 3C. We see that all of the epitaxial layers are continuous, but they are significantly thinner at some points within the trench compared with their nominal thicknesses in Figure 1A. The nominally 200-nm thick GaAs contact layer is 170 and 66 nm at the thickest and thinnest points within this image, respectively. We cannot see any contrast between the GaAs:Zn base and the GaAs:Se emitter, but the emitter presumably exhibits similar thickness variation. Separate cross-sectional SEM imaging of a similar region of non-planarity in this sample taken before processing (Figure 3E) found areas with a void in the epitaxial growth above a trench between facets in which the contact, emitter, and window layers did not completely coat the base layer. We suspect this could lead to a scenario in which the metal is in direct contact with the p-base, forming a Schottky diode.

We measured the external radiative efficiency (ERE) and then simultaneously fit the ERE and dark *I-V*s for devices A and B from Figure 1E as in Geisz et al.[19] to further

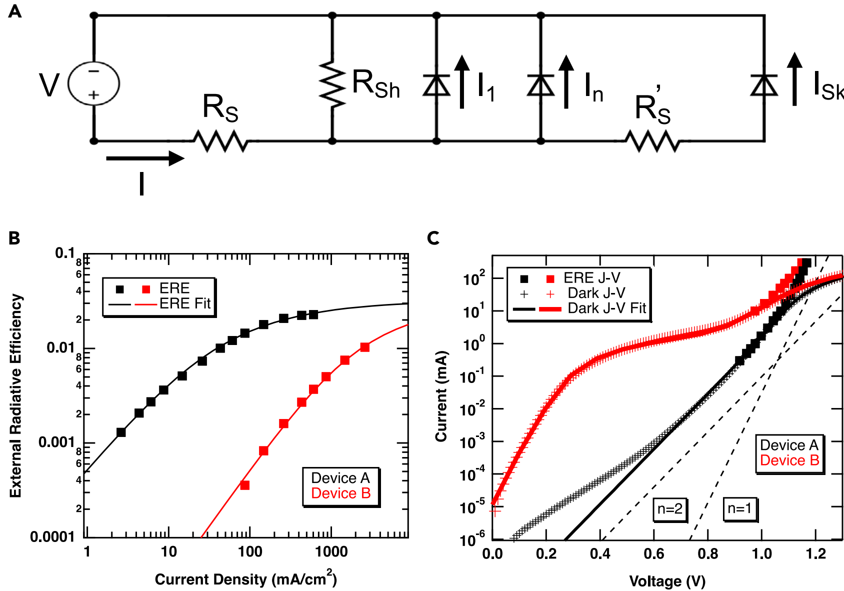

Figure 4. Modeling the device behavior

(A) Circuit diagram describing the 3-diode model used to fit device B.

(B and C) (B) External radiative efficiency and (C) dark *I-V* for device A (non-shunted) and device B (shunted). Data are plotted as crosses and model fits as lines. Dark *I-V* implied from the external radiative efficiency are plotted as square points in (C).

understand the device behavior. We fit device A to the standard 2-diode model[19] and device B to a 3-diode model,[18] illustrated in Figure 4A, containing a third term to account for the non-ideal shunt caused by a possible Schottky barrier diode:

$$I = I_1 + I_n + I_{Sk} \quad \text{(Equation 1)}$$

$$I = I_{01}\left(e^{\frac{q(V-IR_S)}{kT}} - 1\right) + I_{0n}\left(e^{\frac{q(V-IR_S)}{nkT}} - 1\right) + \frac{V - IR_S}{R_{sh}} + I_{0Sk}\left(e^{\frac{q\left(V-IR_S-I_{Sk}R_S'\right)}{n_{Sk}kT}} - 1\right) \quad \text{(Equation 2)}$$

Where I_1, I_n, and I_{Sk} are the currents through the model diodes with unity ideality, n ~ 2 ideality, and the shunt/Schottky diode, respectively. I_{01}, I_{0n}, and I_{0Sk} are the diode saturation currents of those diodes, respectively, R_S and R_{sh} are the main series and shunt resistances, respectively; R_S' and n_{Sk} are the resistance and ideality of the Schottky diode, respectively, and the other variables have their usual definitions. We use current instead of current density due to the difference in areas between the two diode regions. Whereas the traditional n = 1 and n ~ 2 diodes have the 0.116 cm^2 area defined by the mesa isolation during processing, the area of the shunted regions is much smaller and unknown, confined to the immediate area near the specific defect(s).

Figures 4B and 4C show the results of the ERE measurements and the dark *I-V* measurements, respectively, along with fits to the data by eye. The square points in Figure 4C are the implied dark *I-V* calculated from the ERE. The fit parameters are given in Table 1. We see that the three-diode model provides a reasonable fit to device B (see Figure S1 for sensitivity analysis of select parameters), which exhibits the non-linear shunt. The two devices have a similar I_{01} saturation current within ten percent of each other, but device B has a significantly higher I_{0n} current, implying that the non-linear shunt may be accompanied by other defects that increase the

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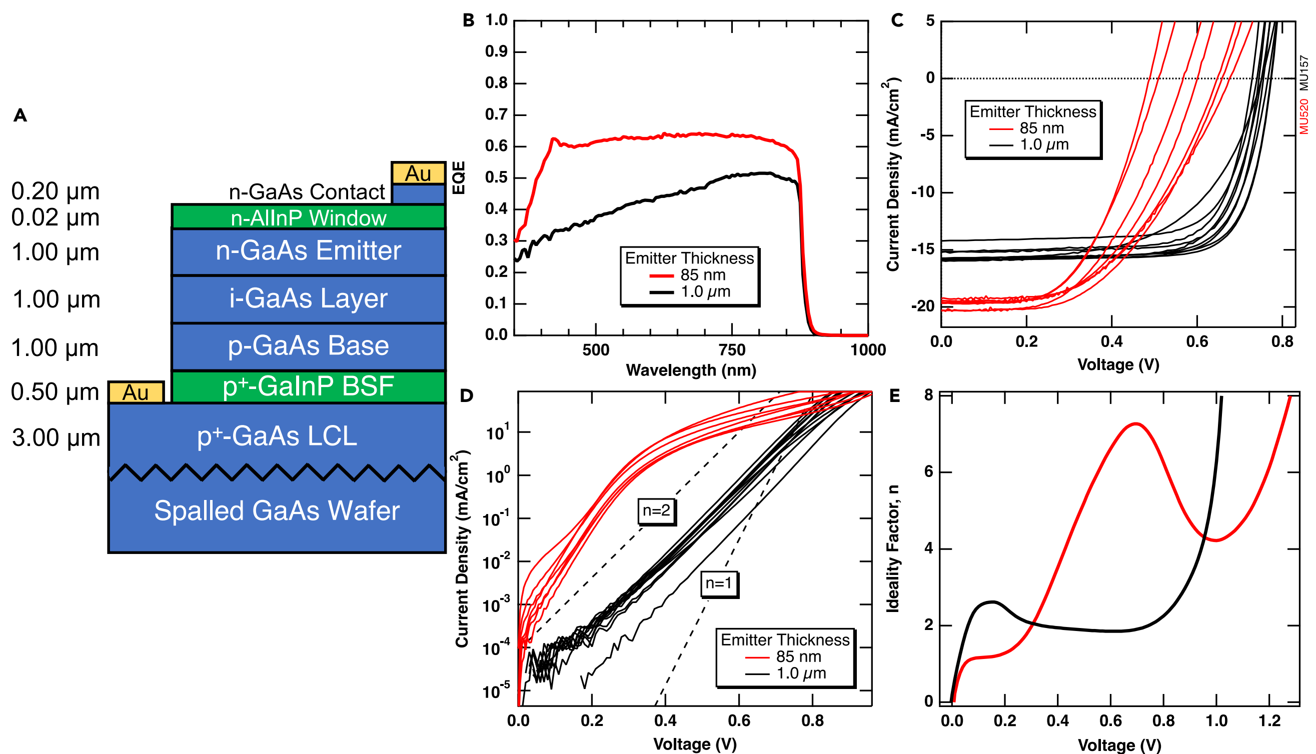

Figure 5. Effect of changing the device structure

Device structure (A), external quantum efficiency (B), light current density-voltage curves (C), dark current density-voltage curves (D) and ideality-voltage curves (E) for devices grown directly on as-spalled substrates with thin or thick emitters.

non-radiative recombination current. The shunt diode has an ideality of 1.2, which is atypical of n-p diodes at low voltage, in which n ~ 2 SRH recombination current normally dominates. We note that this ideality is comparable to values of n ~ 1.2 reported in the literature for metal/p-GaAs Schottky diodes.[20] The series resistance of the shunt diode is over two orders of magnitude larger than that for the n-p diode, presumably because the shunted area is far smaller than that of the surrounding diode. We suspect the resistivities, normalized for their differing areas, are more similar.

Lastly, we studied the effect of the device structure on performance to test whether the potential thinness of the emitter could be responsible for the observed shunt behavior. We grew a device with a n-i-p structure with a 1 μm-thick GaAs:Se emitter, 1 μm unintentionally doped GaAs layer, and a 1 μm GaAs:Zn base layer on an as-spalled SLO substrate without wet etching, as shown in Figure 5A. Figures 5B–5E show the EQE, light *J-V* curves, dark *J-V* curves, and *n-V* curves, respectively, for this device compared with the thin emitter device grown on a separate unetched SLO substrate. The EQE decreases in the thick emitter sample and develops a slope from front to back, suggesting that the carrier diffusion length in the emitter is not sufficiently large to sustain efficient carrier collection in a 1-μm-thick emitter. We attribute this decrease to the unoptimized doping density in the thick emitter. We see a significant increase in the open-circuit voltage in the light *J-V* curves, despite the reduced carrier collection in the emitter. Furthermore, looking at the dark *J-V*, none of the curves in the thick emitter devices exhibit the shunted *J-V* behavior observed in the thin emitter device. All of the devices exhibit an n = 2 slope, indicating that the dark current is limited by SRH recombination in the depletion region,

Table 1. Parameters used in dark *I-V* fitting in Figure 4

Parameter	Device A (non-shunted)	Device B (shunted)
I_{01} (mA)	3.6×10^{-18}	3.8×10^{-18}
I_{0n} (mA)	5.0×10^{-9}	2.9×10^{-7}
I_{0Sk} (mA)	–	1.9×10^{-5}
R_S (Ω)	1.5	1.6
R_{Sh} (Ω)	90,000	90,000
R'_S (Ω)	–	241
n	2.0	2.2
n_{Sk}	–	1.2

likely attributable to the thick i-layer placed between the emitter and base. Looking at the *n-V* plot, the thick emitter device does not exhibit the peak signature of the shunted thin emitter device, suggesting that the thicker emitter has solved the shunting issue.

DISCUSSION

The data shown in the previous section suggest that growth over rough, faceted substrates does not inherently decrease epitaxial material quality but does present some pitfalls that must be avoided to maintain device performance. The fact that the EQE of devices grown on epi-ready and SLO surfaces was nearly equal suggests that the minority carrier diffusion length, one indicator of material quality, was not significantly degraded by growth on the spalled substrates. However, the drastic decrease in V_{OC} and peak in the *n-V* curve suggest some other problem with the devices leading to increased recombination. The signature of a peak in a solar cell's *n-V* curve was previously observed in buried contact Si solar cells in which the n-type diffusion doping in the contact trench was not sufficient to convert the p-type base material in the wafer to n-type.[21] When the grid fingers were deposited in the trenches, the grids contacted the base directly, forming localized Schottky barrier contacts with an enlarged diode saturation current and a high resistance due to the relatively low contact area.[18] This scenario produced a *n-V* characteristic similar to that observed in the non-linearly shunted GaAs device B shown in Figure 1E. At low voltage, the dark *I-V* was dominated by the Schottky diode with an ideality of $1 > n > 1.5$, but then the ideality increased significantly above $n = 2$ with voltage as the series resistance losses at the Schottky diode dominated the *I-V* behavior. Then, as voltage was increased further, the larger area semiconductor n-p diode turned on and dominated the *I-V* behavior, causing a peak in the *n-V* curve as the ideality decreased back to $n \sim 1–2$ as expected for the main semiconductor diode. This behavior is precisely what we see in the DLIT data in Figure 2, in which the current is localized at the non-linear shunts observed in the images at moderate voltages. Although we did not identify direct evidence of the contact metal directly contacting the p-GaAs base, we did observe trenches in other regions where the growth was disrupted, and the base was not coated by the emitter. If the contact metal were to fill one of these trenches and contact the base, it could cause the observed behavior by forming a Schottky diode. The fact that we obtained a best fit to the dark *I-V* of the device B device using an ideality of 1.2 for the shunt diode provides support for this explanation because Schottky diodes on p-GaAs were previously reported to exhibit ideality factors of $n \sim 1.2$.[20] Alternatively, if the window layer is too thin in a region where the epitaxy is disrupted, as shown in Figure 3D, it is possible that that situation could cause a localized region of poor passivation with a higher saturation current. On the other hand, the results of the experiment

shown in Figure 5 suggest that the problem is indeed the formation of a Schottky contact, because we did not alter the thickness of the window, yet thickening the emitter eliminated the non-linear shunting behavior observed in the thin emitter devices. Thus, it is plausible to assume that, despite the possible formation of trenches in the epitaxial layers as in Figure 3E, thickening the emitter created a scenario in which the p-GaAs base material at the bottom of the trench was sufficiently coated with n-GaAs to prevent the formation of a Schottky diode.

The presence of these localized, non-linear shunts presents a potential failure mode in devices grown on acoustically spalled substrates, reducing their V_{OC} and, by extension, efficiency, although the material quality is generally high in most of the epitaxial material. The question becomes how to mitigate or prevent the formation of these non-linear shunts to maintain a high V_{OC}. The results of this study present a few potential solutions. First, reducing the feature height on the SLO surfaces should improve device performance. We note that a peak-to-valley height of 2–3 μm was enough to disrupt the epitaxial growth process and create shunts, meaning that features below this size should be targeted. We expect further tuning of the SLO process to lead to flat surfaces (sub-2-μm facets) across the entire wafer. Evidence of such surfaces is presently observed in many areas of the wafers described in this work, as depicted in the cross-section SEM image in Figure S2. Spalling of substrate orientations with low fracture energy planes aligned to the surface, such as (110), is also a way to reduce feature height generated by the spall.[22] Post-spall planarization is another option. The results in Figure 1 show that wet etching of the spalled substrates before growth eliminated the shunting issues in most of the devices on the sample. NH_4OH-based etches remove material from (n11)B facets faster than (100),[23] which planarizes the surface because the acoustically spalled substrates exhibited facets with predominantly (n11)B orientation (see experimental procedures for more detail). We note that some devices on the wet-etched SLO sample still exhibited signs of non-linear shunting, implying some of the remaining features were still too large. However, there is significant room to optimize the wet etching process. Growth-based planarization is another potential method to reduce the feature size. There is an extremely large parameter space of growth conditions and materials to be explored to attempt to planarize the surface before deposition of the thinner, critical device layers, but there is already evidence in Figure 3C that growth, in particular the growth of GaInP, acted to planarize the valley between two facets.

As an example of how to combine etching and growth-based planarization, we grew the front-junction device structure in an inverted fashion with a 2.0 μm GaInP etch stop/planarization layer, as shown in Figure 6A. This layer is 1.5 μm thicker than the etch stop traditionally employed in our inverted devices grown on epi-ready substrates. This device stack was grown on a piece of SLO substrate etched in the 2:1:10 solution for 3 min. Three devices were processed with one-sun grids and were 0.25 cm^2 in area, and a bilayer ZnS/MgF_2 anti-reflection coating was applied. Figures 6B–6D show the EQE, light *J-V*, and dark *J-V* of these devices, respectively. The collection is excellent, approaching unity as shown in the EQE. The light *J-V*s exhibit a V_{OC} just over 1.06 V, and the dark *J-V*s exhibit no signs of non-linear shunting. We note that this V_{OC} is higher than for the upright devices shown previously in Figure 1, likely because photon recycling is enhanced by the reflective Au rear contact.[24] The best device reached an efficiency of 26.9% $\pm$ 0.2% under the AM1.5G spectrum, as certified by NREL's Cell and Module Performance (CMP) team (see Figure S3). A more in-depth study of planarization via organometallic vapor phase epitaxy (OMVPE) growth is underway, but this result highlights the promise of combining growth planarization with etching planarization to enable high efficiencies on SLO surfaces.

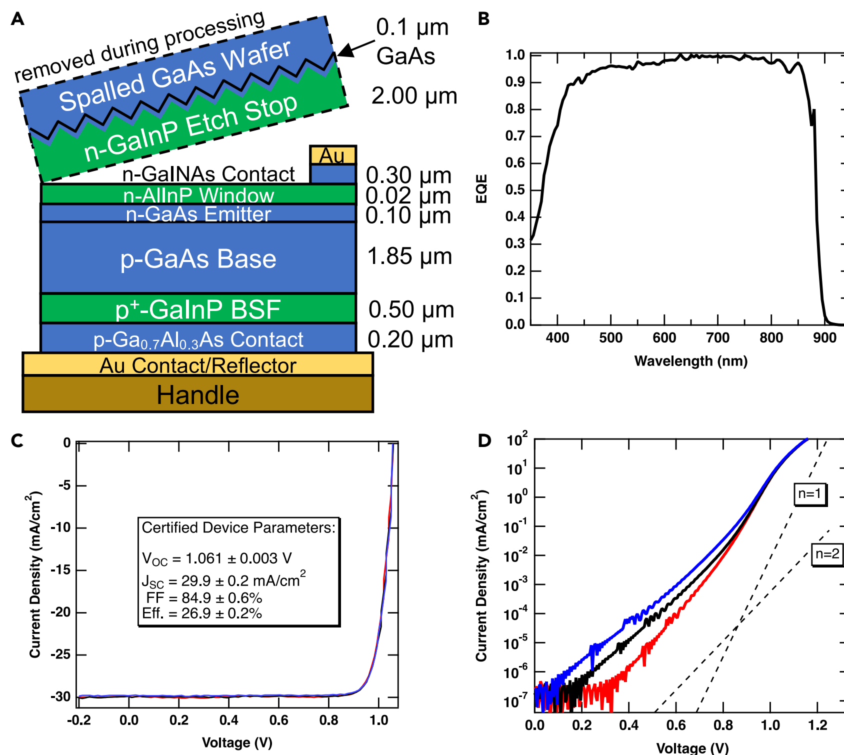

Figure 6. Inverted device grown on acoustically spalled substrate

Device structure (A), external quantum efficiency (B), light current density-voltage curves (C), and dark current density-voltage curves (D) for inverted GaAs solar cells grown on an acoustically spalled surface. One EQE curve is shown, whereas three light and dark *J-V*s with significant overlap are shown.

As a last option, we suggest changes to the device structure as an additional way to mitigate challenges presented by growth on non-planar substrates, assuming that they are suitable for the specific device application. Figure 5 shows that thickening the emitter eliminated signs of non-linear shunting in all the devices on that sample, which was grown on an as-spalled substrate without any etch planarization. Although the EQE decreased due to sub-optimal minority carrier diffusion length in that layer, we note that this parameter can be improved by optimization of the doping density and/or the growth conditions.

In summary, we studied the growth of GaAs solar cells on non-flat, acoustically spalled GaAs substrates as a step toward substrate cost reduction. Growth on these substrates led to the formation of non-linear shunts, which reduced the V_{OC} and efficiency of the devices, although EQE measurements suggested the bulk material quality was not significantly reduced by the presence of spall-related surface facets. The shunts were correlated with disruptions in the epitaxial growth over surface facets with 2–3 μm peak-to-valley height. We presented evidence for the hypothesis that Schottky barrier diodes with poor *J-V* properties formed in places where the metal contact grid was in direct contact with the p-GaAs base layer. We demonstrated that these defects were mitigated or eliminated via planarization of the as-spalled substrate by growth, etching or redesign of the device structure to thicken the emitter layer, achieving 26.9% ± 0.2% efficiency in a device grown on a substrate previously subjected to acoustic spalling. These results enable the epitaxial growth of high-performance devices on potentially lower-cost substrates with μm-scale features.

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EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Kevin L. Schulte (kevin.schulte@nrel.gov).

Materials availability

This study did not generate new unique materials.

Data availability

The data generated in this study are included in the manuscript and supplemental information and will be made available on request.

Substrate preparation

Substrates were Si-doped (100) GaAs with a 6° misorientation toward the Ga-terminated "(111)A" plane. Substrates were acoustically spalled at Crystal Sonic, Inc. The acoustic SLO process is described as follows: First, a thermal stress was applied to the material through a hot/cold plate to a point where the stress intensity factor (K) is close but below the critical stress of the material (K_c) and thus insufficient to initiate spontaneous cracking of the material. A small indentation is produced using Crystal Sonic's proprietary processes, and subsequently, a controlled ultrasound wave is applied to the material to elevate the total stress applied at a crack tip above K_C. By modulating the ultrasound signal, the crack is then controllably propagated throughout the substrate.[15] As shown in previous work[13] the applied stress field at the crack tip, K, can dramatically change the dynamics of a propagating crack during the spalling process because it ultimately controls the crack propagation velocity. As initially proposed by Arakawa and observed in our experiments, ΔK, the difference between the applied K and the critical K_C given by the ultrasound signal modulation in these experiments directly affects the final surface roughness.[25,26]

The cleavage propagated predominantly in a [0–11] direction, yielding surfaces with predominantly As-terminated, or (n11)B-type, facets. Cleaved ¼ pieces of 50-mm-diameter SLO substrates were either subjected to no conditioning and loaded into the reactor "as-spalled" or etched briefly in a 2:1:10 NH_4OH:H_2O_2:H_2O solution to prepare the surface before loading to the growth reactor. This etch is commonly used to remove cleavage dust from substrates created by manual cleavage of full wafers. The etching rate for this mixture is ~1 μm/min on (100) surfaces and is expected to be somewhat higher on (n11)B faceted surfaces.[23] The surface morphology varies somewhat across a given wafer, and Figure 7A presents a laser profilometry height map one of the rougher areas of a surface formed after SLO. A portion of the surface was masked in order to create a step, and the exposed portion of the substrate was etched for 3 min in the 2:1:10 solution, allowing approximate determination of the etching rate. Figure 7B shows some line scans taken from the etched and unetched portions of the surface. Before etching, we see that the surface in this area was covered with regular facets with relatively low peak-to-valley height of 2 μm. It is expected that further improvements to the process will enable flatter surfaces, though these surfaces are already flat enough to obtain high-efficiency devices with minor wet etching and growth planarization. After etching, the facet heights were dramatically reduced, and the valleys between the facets became significantly rounded. The subsequent morphology is consistent with selective etching of the (n11) facets relative to the (100) surface, meaning that the (100) etch rate likely became rate limiting. For a planar (100) surface, we would expect 3 μm of removal after 3 min in the 2:1:10 etchant, which compares nicely to the change in height of the valley bottoms (which gradually present more (100) surface with time).

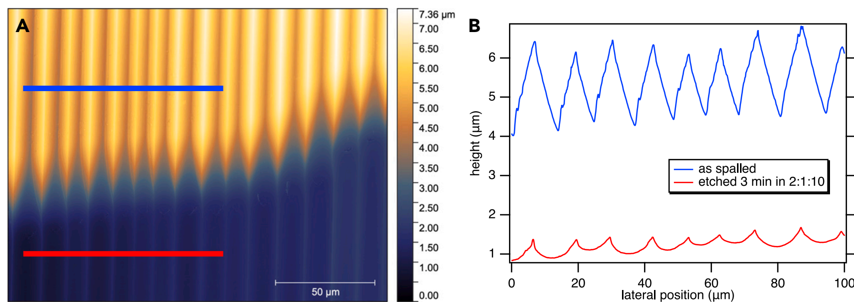

Figure 7. Characterization of the acoustically spalled surface

(A) Height map of a selected SLO surface before and after etching in a 2:1:10 mixture of NH_4OH:H_2O_2:H_2O for 3 min. The upper portion of the sample in the image was masked to preserve it in an unetched state.

(B) Line scans of height vs. lateral position of as-spalled and etched regions of the surface indicated by the blue and red lines in (A).

Epitaxial growth

All devices were grown by atmospheric-pressure OMVPE using trimethylgallium, triethylgallium, trimethylindium, trimethylaluminum, arsine, and phosphine precursors. Disilane, hydrogen selenide, diethylzinc, and carbon tetrachloride were used as dopants. Upright solar cell devices with one of two structures were grown on previously spalled SLO substrates: either a front junction n-on-p device (Figure 1A) with GaAs:Se emitter thickness of 0.085 µm and a 3-µm GaAs:Zn base, or a n-i-p structure (Figure 5A) with a 1-µm-thick Se-doped emitter, 1 µm thick unintentionally doped layer, and a 1-µm-thick GaAs:Zn base. All of the upright devices were left on wafers. Control devices were grown on a mirror-polished, epitaxy-ready substrate with a 0.085-µm emitter and a 3-µm base. For all upright devices, a 3-µm p-type LCL that served as the back contact layer was deposited first, followed by a 0.5-µm GaInP:Zn back surface field layer, and then the GaAs device layers. Lastly, a bilayer 6/14 nm GaInP:Se/AlInP:Se window layer and delta-doped GaAs:Si front contact layer were deposited. An inverted version of the front-junction device was also grown, as shown in Figure 6A. This device has 2.0 µm GaInP:Zn etch stop layer grown immediately after a 0.1 µm GaAs nucleation layer and uses a $Ga_{0.97}In_{0.03}N_{0.01}As_{0.99}$:Se front contact layer.

Device processing

After growth, the upright devices were processed with a concentrator grid pattern using standard lithography techniques. Excluding the bus bar area, the illuminated area was 0.100 cm^2, whereas the total device area was 0.116 cm^2. Current density measured in the light was calculated using the illuminated area, whereas current density from measurements in the dark was calculated from the full device area. For the upright devices, an Au back contact was electroplated onto the GaAs:C LCL, and an Ni/Au front contact grid pattern was electroplated onto the GaAs:Si contact layer. For the inverted devices, the broad-area Au back contact was plated first, then the wafer was bonded Au side down to a Si handle using epoxy. We note that the Au back contact also serves as a reflective back mirror, potentially enhancing photon recycling and the V_{OC} of these inverted cells.[24] Next, the substrate was selectively etched away, followed by the GaInP etch stop. Then one-sun Ni/Au front grids were plated, and devices of 0.25 cm^2 area were isolated. The grid area was approximately 2% of the total area. A bilayer ZnS (45 nm)/MgF_2 (95 nm) anti-reflection coating was applied to the front surface of the inverted device via thermal

evaporation. For all devices, device area was defined using mesa isolation via photolithography and selective wet etching.

Device characterization

EQE was measured as a function of wavelength on a calibrated instrument using a white light source and a grating monochromator. Current density-voltage (*J-V*) curves were measured from the devices in the dark and in the light under a simulated AM1.5G spectrum that used a XT-10 system with a Xe-arc lamp. The spectrum was set using a GaAs reference cell fabricated, calibrated, and certified at NREL on 9/4/20. The spectral mismatch between the test devices and the reference was 0.5% or below. Cells were measured in the open air at 25°C on a temperature-controlled vacuum hold-down stage. Cells were measured from forward to reverse bias in voltage increments of 5 mV. The dwell time was approximately 100 ms at each voltage. A select device *J-V* was certified by the NREL's CMP team. The CMP team's GaAs reference was last calibrated on 12/28/22. J_{SC} measured their system to be within 0.7% (relative) of the value measured on ours. Electroluminescence ERE was measured on select devices as a function of injected current, as in Geisz et al.[27] Dark *J-V* curves were calculated as a function of injected current using the voltage computed from the ERE using the reciprocity theorem.[28] DLIT images were collected from select devices using a Cedip Silver 660M (FLIR SC5600-M) InSb camera with a lock-in data acquisition rate of 2.4 Hz. Plan-view and cross-sectional SEM images were taken of select samples. Cross-sectional images were taken either of cleaved surfaces or with a dual-beam SEM/FIB instrument after FIB milling to expose the cross-sectional surface in a specific region of interest.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.joule.2023.05.019.

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AUTHOR CONTRIBUTIONS

Conceptualization, K.L.S., M.I.B., E.L.W., and M.A.S.; methodology, K.L.S.; formal analysis, K.L.S. and M.A.S.; investigation, K.L.S., S.W.J., A.K.B., J.T.B., A.N.N., W.E.M., M.Y., and P.G.C.; writing – original draft, K.L.S.; writing – review & editing, all authors; supervision, K.L.S., M.I.B., E.L.W., and M.A.S.; funding acquisition, M.A.S., E.L.W., and M.I.B.

DECLARATION OF INTERESTS

M.I.B. and P.G.C. are inventors of US patents 10,828,800 B2 and 11,504,882 B2, both titled "Sound-assisted crack propagation for semiconductor wafering."

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