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RESEARCH ARTICLE

Cross-sectional mapping of hole concentrations as a function of copper treatment in CdTe photo-voltaic devices

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ABSTRACT

The carrier density and carrier density distribution within CdTe solar cells were studied with scanning capacitance microscopy (SCM). The CdTe solar cells were studied after every process step and as a function of varying copper treatment conditions. It was found that the CdTe film is practically undoped after deposition and after $CdCl_2$ treatment, while after the copper step the carrier density distribution is non-uniform with a mixture of *p*-type and intrinsic grains in the CdTe film. These SCM observations were also confirmed with device performance data as well as capacitance–voltage measurements and Van der Pauw Hall measurements. Copyright © 2014 John Wiley & Sons, Ltd.

KEYWORDS

solar cells; CdTe; scanning capacitance microscopy; carrier density

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1. INTRODUCTION

In recent years, the efficiency of CdTe solar cells has increased rapidly from 17.3% [1] to >20% [2]. This increase in efficiency has been mainly accomplished by improving the fill factor (FF) and the current density (J_{sc}). The open-circuit voltage (V_{oc}) has been relatively constant since the early 1990s [3], and this constant V_{oc} might be a limiting factor from reaching >24% efficiency levels for CdTe-based devices. Important factors that contribute to the V_{oc} include the carrier lifetime, the carrier density, and Fermi-level pinning defects that could occur on grain boundaries or the front/back interface. Recently, Gloeckler *et al.* [4] demonstrated that the carrier lifetime for the best devices is now significantly high such that it should not be a limiting factor anymore [5]. However, the carrier density for high efficiency devices is still relatively low [6] and thus could be considered a potentially limiting factor for V_{oc} improvements.

Mapping the carrier density distribution of photo-voltaic (PV) devices in cross section is a direct way to determine the location of internal junctions and to identify subsurface layers and features. This can reveal the microscopic origin of macroscopic device behavior that is relevant for thin-film devices. Scanning capacitance microscopy (SCM) is a powerful method for mapping dopant variation in semiconductor and photovoltaic devices [7–13] and can thus be utilized to better understand the operation of thin film PV devices. The technique can provide valuable information on carrier density, carrier density gradients, as well as the type of majority carriers within the various layers of the PV device. SCM has been successfully applied to CdTe technology [11–13], to better understand the role of grain boundaries [11,13] and the properties of the CdS window layer [12]. The conclusions of the previous work were that grain boundaries seem to be *n*-type in character and that the carrier density in the CdS component of these devices is too low to actively act as the *n*-type counterpart of the *p*-type CdTe.

In this paper, SCM has been utilized to study the carrier density in the CdTe component of a CdTe photo-voltaic device with the focus on the CdTe grains. The impact of the various steps of the device fabrication process was studied, and special focus was placed on the copper treatment step and its effect on the doping of the CdTe film. SCM data is compared to device performance data and data obtained from capacitance–voltage (CV), drive-level capacitance profiling (DLCP), as well as Hall measurements.

2. EXPERIMENTAL DETAILS

2.1. Device fabrication and sample preparation

Devices are fabricated on thin glass (1.4 mm thick, Asahi PVN++) coated with cadmium-stannate (CTO) as a transparent conductive oxide (TCO) and Zn-doped tin-oxide (ZTO) as a buffer layer. The TCO and buffer are obtained from large sheets of glass coming from a large area production tool, guaranteeing good part-to-part reproducibility. The sheet resistance of the TCO is 4.0 ± 0.2 Ohm/sq., while the buffer layer has a carrier density of $\sim 2 \times 10^{18}\,\mathrm{cm}^{-3}$. Samples with a size of $3.8 \times 3.8\,\mathrm{cm}^2$ ($1.5'' \times 1.5''$) are mechanically scribed from glass sheets. Each substrate was manually scrubbed for 10 s per side using a nylon brush dipped in a surfactant solution (Valtron® SP2200 diluted to 1% in deionized (DI) water). After the surfactant scrub, the substrates were held standing vertically in a Teflon carrier submersed in DI water. The batch was then put into an automated rinser–drier tool where it was rinsed with DI water and spun dry with heated N_2. The samples were stored in a nitrogen purged dry-box after cleaning.

Sputter deposited CdS, with a thickness of approximately 90 nm, was used as an n-type window layer. CdTe was deposited using close-space sublimation (CSS) [e.g. 14]. Samples with CdS were mounted with the CdS facing down over a CdTe source pellet (99.999% purity). During a 10-min pump-down to below 7 Pa, the substrate and the source were heated to about 200 °C to burn off residual water vapor from the surface. The chamber was filled with 2000 Pa of helium and 130 Pa of oxygen, resulting in a helium atmosphere with ~6% of oxygen. After this step the source and substrate were heated to 625 °C and 550 °C, respectively, using infra-red lamps. The spacing between the source and substrate was ~2 mm, which provided a constant substrate temperature during the deposition step. It has been observed that decreasing this spacing will cause the substrate temperature to increase during deposition, due to heating from the source. Typical growth rates were approximately 1 μm/min, which provided good thickness control. The CdTe films were deposited to a thickness of approximately 3 μm. This is significantly thinner than thickness' reported for typical historical record cell devices [3,15], and was considered to be a more manufacturable thickness in light of concerns regarding tellurium availability [16,17].

After CdTe deposition the samples were treated with a $CdCl_2$ (99.99% purity) solution. The solution was prepared by dissolving $CdCl_2$ powder (100 g/l) in water (20%) and methanol (80%). The solution was applied to the CdTe surface and allowed to dry. The samples were annealed in a furnace for 20 min at ~400 °C and after cool-down the remaining $CdCl_2$ was rinsed off. At this point in time, the minority carrier lifetime is established (see also [18]). After the rinse, the CdTe sample was submerged in a solution that contained 0.8 g/l of Cu-acetate, after which they were baked in a furnace. The anneal time and temperature have been varied for the data discussed in the paper. Rough cell outlines were defined by laser scribing to the TCO layer. The whole surface was then covered with a thin layer of Au (~100 nm) using evaporation, including the areas where the TCO was exposed by laser scribing. After gold deposition, four $1 \times 1\,\mathrm{cm}^2$ cells were formed within the rough cell outlines. More information on the fabrication process can be found elsewhere [19], and the data presented in this paper is the average of the four cells. Curves of current vs. voltage were measured using a four-point probe setup, using standard AM-1.5 conditions at 25 °C. After cell testing, CV/DLCP measurements were performed. Once the measurements were completed, a cell from each condition was cleaved and analyzed by SCM.

Samples for van der Pauw Hall measurements were prepared in parallel with the devices. The TCO and buffer layer were omitted from the process, and 20 nm of CdS was deposited directly on glass to promote adhesion of the CdTe to the glass surface. If the TCO and buffer are present, or if thicker CdS is used, the Hall measurements will indicate *n*-type films with the carrier density of the underlying structure. At 20-nm CdS, the CdS layer was completely dissolved within the CdTe layer during the CdTe deposition step. After CdTe deposition, the films were exposed to the same treatments as the full device structures and then prepared for Hall measurements. This included cutting the CdTe samples into $1 \times 1\,\mathrm{cm}^2$ squares and the placement of graphite contacts (Electrodag 440B from Acheson) at the corners of the samples. The graphite was cured by placing the samples on a hot plate maintained at 160 °C for 10 min in air. Once the contacts were cured, and the samples had cooled down, the pieces were mounted on a customized Hall probe card with four tungsten probes that made an electrical connection with the four graphite contacts. The probe tips also held the samples securely to the probe card, and the measurements were performed in the dark. The sheet resistance was measured using the van der Pauw method [20]. The van der Pauw measurements were followed by measuring the Hall voltages in the presence of a magnetic field perpendicular to the plane of the sample and whose magnitude was maintained at 2.0 T. The Hall voltage was used to calculate the carrier mobility as well as the sheet carrier density. To obtain the carrier concentration, the sheet carrier density was divided by the thickness of the film, which was determined through spectroscopic ellipsometry and verified by cross-sectional scanning electron microscopy. The van der Pauw Hall measurements were conducted using a LakeShore 7600 Series Hall system.

Seven samples were prepared for the study presented in this paper. Table I lists the steps that are performed on each sample after the CdTe deposition step, excluding the scribing and contacting steps. This set of samples explores the impact of the various process steps on the carrier density, with special focus on the Cu-treatment. Standard conditions for the copper treatment were 210 °C for 12 min. The lower temperature explored the effect of under-treatment, and the longer times at 250 °C were

Table I. Samples used in this study and back-end process applied to those samples.

Sample	Process
A	CdTe
B	CdTe + $CdCl_2$
C	CdTe + $CdCl_2$ + Cu (170 °C for 12 min)
D	CdTe + $CdCl_2$ + Cu (210 °C for 12 min)
E	CdTe + $CdCl_2$ + Cu (250 °C for 12 min)
F	CdTe + $CdCl_2$ + Cu (250 °C for 18 min)
G	CdTe + $CdCl_2$ + Cu (250 °C for 30 min)

performed to understand the effect of over-treatment. Time was chosen as a variable instead of higher temperatures, because the devices were shunted at higher temperatures.

2.2. Scanning capacitance microscopy

In SCM, a conducting atomic force microscopy (AFM) tip is used to scan the surface in contact mode (Figure S1, supporting information) [7]. The sample surface formed a native oxide layer, which resulted in a metal–insulator–semiconductor structure between the tip and the sample surface. Simultaneous with the topography data collection, an AC-bias is applied to the sample while the tip is grounded. The resulting oscillation of carriers near the tip leads to a modulated capacitance (dC/dV), which is measured by a high-sensitivity capacitance-sensing circuit, using a lock-in amplifier (Figure S1, supporting information). The capacitance measured by the SCM sensor varies as the carriers move towards (accumulation) and away from (depletion) the probe. When the sample is fully depleted the measured capacitance is that of the oxide plus the depletion layer. When carriers are accumulated at the surface, the measured capacitance is that of the oxide layer. This capacitance variation in response to the tip-applied field forms the basis of the SCM measurement. The magnitude of the change in capacitance (dC) for a given change in voltage (dV) depends on the carrier concentration. For heavily doped materials the carriers do not move far. Hence, the measured capacitance variation between accumulation and depletion is small. The opposite is true for lightly doped semiconductors which yield a large capacitance change. The sign of the measured dC/dV signal changes between *n*-type and *p*-type. In *p*-type semiconductors, as the sample voltage becomes more negative relative to the tip, the width of the surface depletion layer will increase, leading to a decrease in total capacitance. If the sample voltage is positive, accumulation will occur, and the capacitance measured will be that of the oxide layer only. For *n*-type samples the effects are opposite [7]. The SCM imaging in this study were performed with a Dimension 3000 equipped for SCM (Veeco Metrology Inc., Santa Barbara, CA). The analyses were performed in contact mode, in air, using 9-kHz, 0.8-N/m RMN-12PT300B platinum tips (Bruker nano Inc., Camarillo, CA).

The samples in Table I were mapped in cross section. The cleaved cross sections of the CdTe devices were prepared by scribing the film side of the sample, followed by cleaving the CdTe film side under tension and the glass side in compression [12] using a set of glass run pliers. The cleaved cross sections were not smoothed further, either mechanically or chemically, to prevent the introduction of extraneous surface defects that might affect the electronic properties. Figure S2 (supporting information) shows that the cleave breaks mainly through grains rather than along grain boundaries. In many cases, the fracture appears to travel along certain crystal orientations, as the fracture is very linear across certain grains.

3. RESULTS AND DISCUSSION

3.1. Device results

Figure 1a shows the efficiency for the various devices as listed in Table I. It is clear that devices without any treatment have very poor efficiency. Devices with 10% efficiency can be achieved after the $CdCl_2$ treatment; however, Cu is necessary for higher efficiency devices. The data also shows that annealing the CdTe for 12 min at 170 °C, after applying the Cu, is not enough. Devices with efficiencies greater than 14.5% were achieved by annealing for 12 min at either 210 °C or 250 °C. Annealing for longer than 12 min at 250 °C decreases the performance of the devices.

From the perspective of the second-level metrics of the devices (Figure 1b and c) it is clear that the trend observed for the efficiency (Figure 1a) was also present for the open-circuit voltage (V_{oc}) and the fill factor (FF). Devices without Cu have similar V_{oc} values of ~650 mV, whereas devices with anneal conditions of 210 °C or 250 °C for 12 min had V_{oc} values greater than 830 mV. The latter two conditions also had the highest values for FF. Devices without the $CdCl_2$ treatment had very poor FF. Further explanation of this will be discussed later.

Figure 1d shows the J_{sc} of the various devices, except for the device without the $CdCl_2$ treatment. The low FF for this device resulted in much lower J_{sc}, primarily due to large voltage-dependent current collection. The remaining devices show an interesting downward trend with increasing Cu-treatment. A possible explanation of this effect could be that at longer treatment times at 250 °C, Cu-related recombination centers were formed within the CdTe layer. This was supported to some extent by the quantum efficiency curves (Figure 2a) for these devices, where the highest J_{sc} values corresponded to the largest areas under the quantum efficiency curves. It was also clear that lower J_{sc} values were coming from poorer collection in the red, indicating possibly more recombination towards the back of the CdTe film.

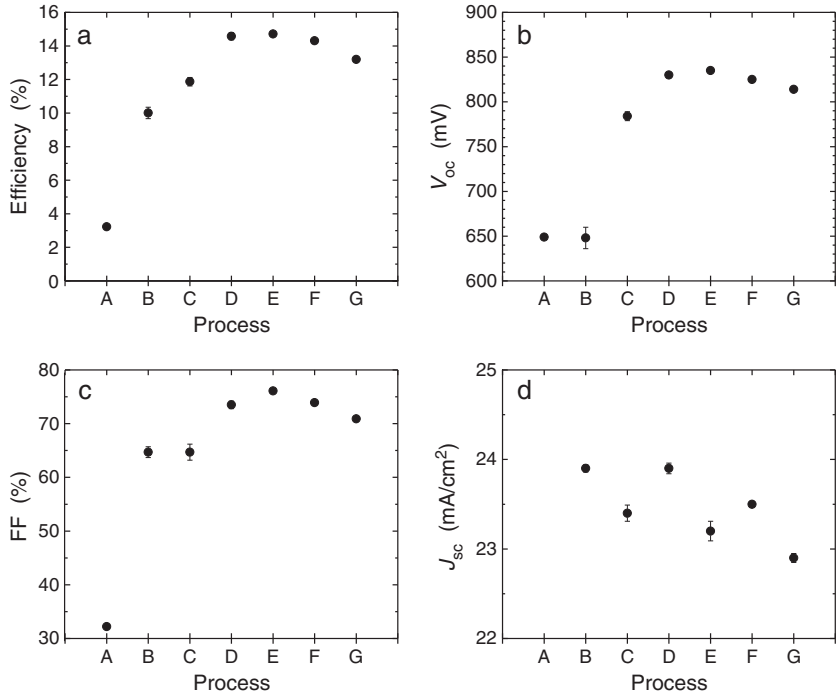

Figure 1. (a) Efficiency, (b) open-circuit voltage, (c) fill factor, and (d) short-circuit current density of the various devices as listed in Table I. In the J_{sc} graph the device made using untreated CdTe is omitted because it has significantly lower J_{sc} due to large amount of voltage dependent current collection.

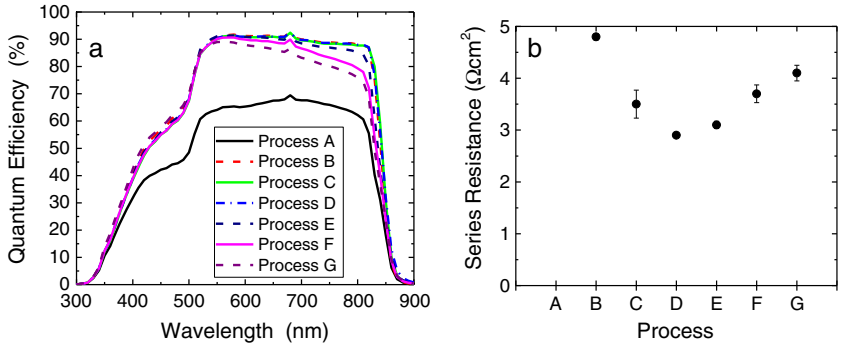

Figure 2. (a) Quantum efficiency curves at 0 V and (b) series resistance at open-circuit for the various devices as listed in Table I. In Figure 2a, the data for process A is the bottom line, the data for process B, C, and D are overlapping, while for process E to F to G more and more loss in the red is observed. The data for untreated CdTe is omitted for clarity from Figure 2b, because the series resistance of that device is significantly higher.

Closer inspection of the FF trend (Figure 1c) revealed that it was mainly driven by the series resistance (Figure 2b), whereas the shunting resistance was relatively constant for all devices except for the sample without a $CdCl_2$ treatment (not shown). The device without the $CdCl_2$ treatment also had much higher series resistance and was omitted from the graph. The figure clearly shows that the devices with the lowest series resistance also had the best FF and that optimizing the Cu treatment maximizes the V_{oc}, resulting in the highest efficiency. The optimum FF is probably related to the back-contact resistance, while the optimum V_{oc} is likely related to optimized carrier density.

3.2. SCM results

Scanning capacitance measurements were performed on cross sections of the same devices as discussed above. Figure 3 shows the cross-sectional AFM and SCM images

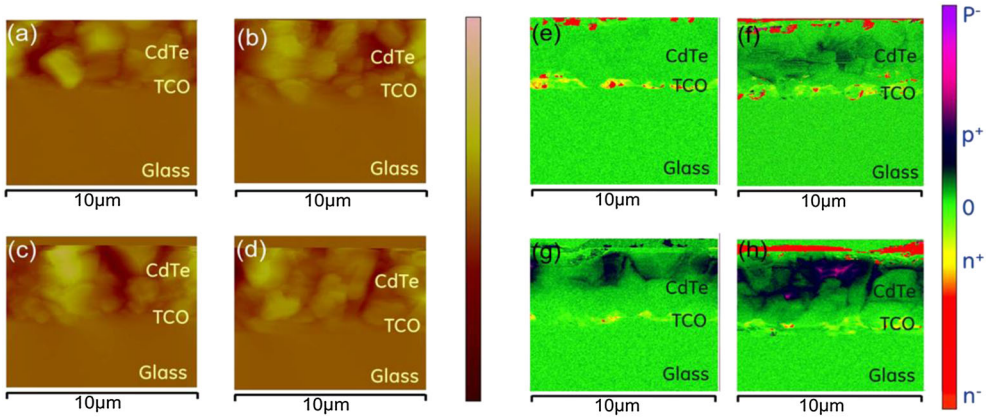

Figure 3. (a–d) 10 × 10 μm AFM topography images and (e–h) 10 × 10 μm SCM images taken simultaneously of four cross section of CdTe/CdS solar cell at different stages within the device fabrication process. (a) and (e) as deposited CdTe; (b) and (f) only $CdCl_2$; (c) and (g) low temperature Cu treatment (170 °C for 12 min); (d) and (h) standard process (210 °C for 12 min).

of as deposited CdTe that was not treated, CdTe that was treated only with $CdCl_2$, CdTe that was exposed to $CdCl_2$ and a low temperature Cu anneal, and CdTe after $CdCl_2$ with a standard Cu anneal. The AFM images show typical topography of CdTe for the four samples, which more or less show the same features. However, the SCM images reveal a significant difference of the *p*-type distribution in the CdTe layer, confirming that the SCM signal is not merely a topographic reproduction. In all images the glass does not give any signal and the CTO/ZTO/CdS stack gives a yellow/red *n*-type signal.

As-deposited CdTe is clearly intrinsic in nature (Figure 3e). Somewhat surprisingly, the $CdCl_2$ treatment (Figure 3f) also shows generally intrinsic grains with some very light *p*-type doping, which is contrary to what is expected based on defect modeling by Wei *et al.* [21], but could be understood in light of work discussed by Marfaing [22]. Annealing a $CdCl_2$ treated sample for 12 min at 170 °C in the presence of Cu results in some *p*-type formation close to the back-contact, but clearly not a complete conversion to *p*-type of the whole CdTe layer, leaving a significant intrinsic CdTe region near the front of the device (Figure 3g). Higher Cu-anneal temperatures were typically required to make good devices. The CdTe layer was significantly *p*-type doped (Figure 3h) after a standard Cu treatment at 210 °C. At the same time, it was clear that the carrier density distribution was not uniform, and grains near the front interface with the CdS still appeared to be largely intrinsic. The *p*-type CdTe layer after the standard Cu treatment forms a *p*–*n* junction at the CdTe/CdS interface, in agreement with Visoly-Fisher *et al.* [12]. The interface between *n*- and *p*-type materials appears rough due to the way the sample cleaved. The top region of Figure 3h shows a smooth region in the AFM image and no signal in the SCM image. This region was beyond the back contact and was caused by the tip moving off the sample. A narrow region on the edge of the cross section generates an SCM signal that can be assigned as *n*-type. However, tip–surface contact in this area may have changed while scanning the edge of the cross section, and therefore the SCM signal may be an artifact.

Figure 4 shows line scans [8,12] that average 1-μm strips across the four sections shown in Figure 3 (e–h). The profile of the untreated CdTe shows that the as-deposited CdTe is intrinsic, as the level in the absorber was the same as for the glass, which could be observed to the right of the *n*-type region. It also shows that the transition to the *n*-type window layer stack occurs at about 3 μm from the back-contact. The CdTe that was treated with $CdCl_2$ shows the appearance of the *p*-type signal near the back contact, and a similar profile is observed for the CdTe that was exposed to a low-temperature Cu treatment (170 °C). The dopant profile of the CdTe after a standard treatment with Cu shows the *p*–*n* transition across the

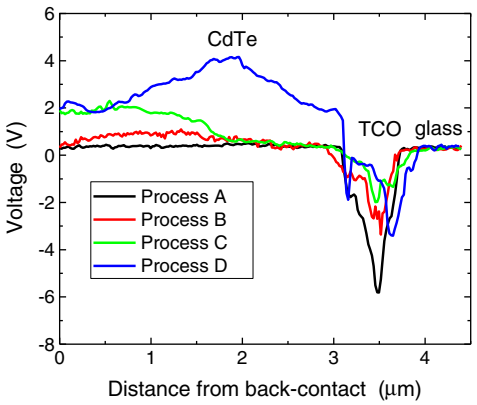

Figure 4. Accumulative voltages obtained by averaging the voltages from the various SCM images as shown in Figure 3 (e–h) as a function of the distance from the physical back-contact of the devices: dark blue—as deposited CdTe; light blue—only $CdCl_2$; green—low temperature Cu treatment (170 °C for 12 min); gray—standard process (210 °C for 12 min).

CdTe/CdS interface. This data representation clearly shows that there is some *p*-type doping after the $CdCl_2$-treatment, but that it is much less than Cu treated samples. It also shows that the Cu-related acceptor states appear to penetrate from the back, as the increase in carrier density is observed in the top half of the CdTe film at 170 °C. Higher carrier density is obtained in the bulk and toward the interface with the CdS when annealed at 210 °C. The peak in voltage, i.e. carrier density, in the middle of the CdTe absorber could be important, but this effect has not been studied.

Figure 5 shows SCM images of the cross sections that were over-treated with Cu at 250 °C for 12 min, 18 min, and 30 min. The only difference between temperatures of 210 °C and 250 °C for 12 min (Figure 3h vs. 5a) appears to be the volume fraction of the CdTe grains that are doped *p*-type. The CdTe device with a treatment temperature of 210 °C still shows a significant amount of intrinsic grains, especially near the front interface, while at 250 °C the grains at the front are mostly converted to *p*-type material. Figure 5 (b–d) shows that the over-treatment with Cu for 18 and 30 min forms a mixture of *n*-type and intrinsic grains near the back contact. This must mean that the Cu_{Cd} acceptor state [21] must be neutralized or over-compensated by other defect states. One way to understand this would be that above a certain Cu_{Cd} density, the formation of this defect becomes less favorable and first neutral Cu_i–Cu_{Cd} complexes are being formed [23,24], which could on some occasions be dominated by Cu_i donor states [21], resulting in *n*-type CdTe grains. Similar observations have also been reported by Ma *et al*. [25]. The fact that the cells still work fine, which would not be obvious from looking at the images of Figure 5, could probably be explained through understanding that there might still be areas

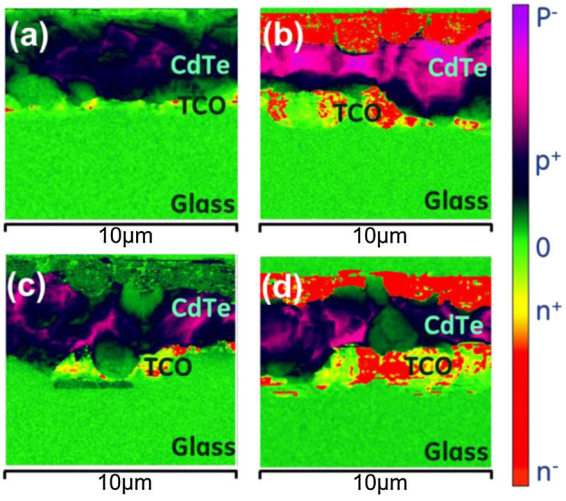

Figure 5. 10 × 10 μm SCM image of the cross sections for CdTe devices that were over-treated with Cu: (a) annealed at 250 °C for 12 min, (b) annealed at 250 °C for 18 min, and (c) and (d) annealed at 250 °C for 30 min.

where *p*-type CdTe is in contact with the back-contact, making the *n*-type and intrinsic regions near the back-contact inactive from a device perspective. The increased path created by channeling holes through *p*-type grains to the back-contact should result in an increase in series resistance, consistent with the data shown in Figure 2b.

3.3. Other device-related characterization

A complementary technique to understand the carrier density in the CdTe film is CV/DLCP. Figure 6a shows a carrier density profile as extracted from DLCP. For devices without any treatment of the CdTe it is hard to get any meaningful signal from CV/DLCP, and only some field near the back-contact can be observed, likely due to the small diode formed between intrinsic CdTe and the Au back metal. Upon treating the sample with $CdCl_2$, followed by Cu-annealing at 170 °C, one can start to see meaningful CV/DLCP data, especially near the back-contact. The CdTe layer is fully depleted with these conditions (Figure 6b). The CV/DLCP profiles reach from the front to the back on the sample with a 12-min anneal at 210 °C, and a U-shape is observed. The electrical thickness is close to the physical thickness of these devices. Higher temperature and longer treatment times pushed the carrier density increasingly toward the front of the device, and now only a meaningful signal from CV and DLCP can be extracted near the front-contact of the device. This indicates, from a capacitance perspective, that the back-end of the devices are inactive and only contribute to the resistance, which could explain the increase in series resistance with longer Cu anneal times. This agreed with the SCM observations, where the intrinsic and *n*-type regions in the back could be the resistance that prohibits the CdTe layer from being depleted by the bias-voltage (Figure 6b).

Figure 7 shows the carrier density as determined by van der Pauw Hall measurements for samples C, D, E, and G. The Hall measurement data for the Cu-containing devices was taken in the dark. As-deposited and $CdCl_2$-treated CdTe films could not be measured in the dark as they were too resistive to collect meaningful Hall data and are therefore omitted from Figure 7. Devices without any Cu were measured in ambient light, which decreased the resistivity enough to determine a Hall voltage. This decrease in resistivity with light is mainly reflected in increased carrier mobility. In general, even with ambient light the data indicated low carrier density, in line with the SCM data. These measurements on the as-deposited film resulted in *p*-type carrier density of $(2 \pm 2) \times 10^{10}\,cm^{-3}$, while the $CdCl_2$ treated sample resulted in a carrier density of $(2 \pm 1) \times 10^{11}\,cm^{-3}$ and *n*-type behavior, which could be associated with *n*-type grain boundaries [11,13]. The data confirmed that the carrier density is significantly lower, as compared to Cu-doped CdTe. When the CdTe films were treated with Cu, the carrier density starts to increase, reaching typical values slightly above $2 \times 10^{14}\,cm^{-3}$, when annealing at 210 °C and higher. At higher bake

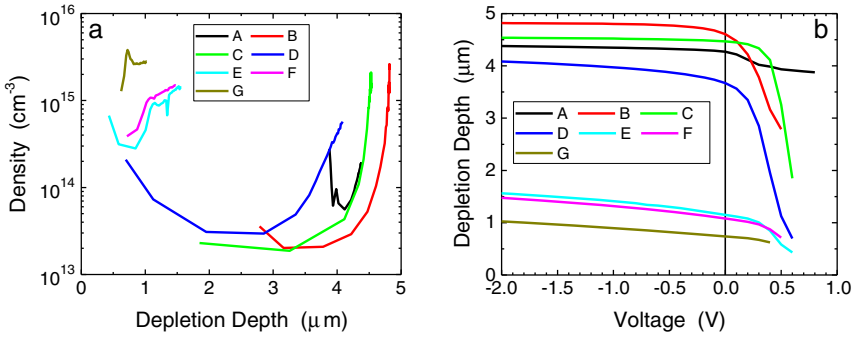

Figure 6. (a) DLCP profiles and (b) depletion depth as a function the bias-voltage of the various devices as listed in Table I.

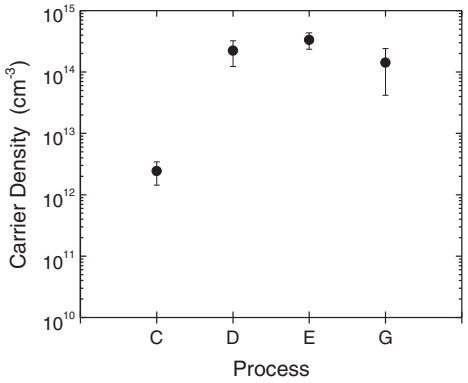

Figure 7. Carrier density as determined through Van der Pauw Hall measurements for CdTe films made according to the conditions A–E and G as described in Table I.

temperature and time, the carrier density does not increase further, with some indication that the carrier density may go down when annealing for 30 min at 250 °C. The latter is in line with what is discussed above and could again be explained by the formation of neutral complexes or compensating donor states. Having these types of regions within the film will effectively decrease the carrier density in the Hall measurements.

4. DISCUSSION AND CONCLUDING REMARKS

The literature has assigned p-type carrier density in CdTe to Cd vacancies and complexes of Cd vacancies with Cl on Te sites [e.g. 21]. The Cu-treatment step is more typically associated with the back-contact formation process [26]. However, in this paper we have demonstrated with two independent techniques that the carrier density in Cu-free CdTe films is very low, to the point that it could be thought of as being intrinsic. This means that during the CdTe deposition step, Cd vacancies, which are proposed to be acceptor states in CdTe [21], were not formed or were formed in combination with compensating donor states. One possible candidate defect that could act as a compensating donor state is the Te anti-site Te_{Cd}, as identified by Berding [27]. The $CdCl_2$ treatment, which is needed to increase the carrier lifetime in CdTe devices [e.g. 18], is typically associated with complexing V_{Cd} with Te_{Cl}, resulting in so-called A-centers, which are supposed to be acceptor states in CdTe [21]. However, the results shown in Figures 3 and 7 indicate that A-centers were not dominant, and if they were formed at all, they were likely compensated with donor states, possibly isolated Cl_{Te} donor states [21]. Marfaing actually discusses that at Cl levels of 10^{18}–10^{19} cm^{-3} one would actually expect *n*-type material, depending on the Cd-vacancy concentration [22]. In that work, the Cd vacancies are actually treated as the compensating states and levels of 10^{14}–10^{16} cm^{-3} would be sufficient to explain the low carrier densities observed in the data shown above. Given the grain-boundary density, these types of densities could easily be obtained. However, the increased resolution of SCM led to the insight that if the charge neutrality is due to compensation, that it happens within the grain. While the Hall data could be explained by *p*-type grains being compensated by *n*-type grain-boundaries, the SCM data actually shows that the charge state of the grains is intrinsic in nature after the $CdCl_2$ treatment, and thus the n-type signal in Hall needs to come from the grain-boundary regions. This is easily understood as Cl mainly populates the grain boundaries [28,29] and the Cl level within the grains are probably low due to very low diffusion coefficients for Cl in CdTe grains [30].

The doping of the CdTe layer in CdTe solar cell devices happens during the Cu step after the $CdCl_2$ treatment, where carrier density seems to be driven in from the back, where the Cu is applied. At 170 °C the CdTe near the back-contact gets lightly doped. Furthermore, the data also illustrates why the amount of Cu in the device needs to be limited, as too much Cu creates compensating defect states. The compensating defect states could over-compensate the preferred acceptor states that are associated with Cu, effectively leaving large parts of the CdTe device inactive. This becomes even more important when the CdTe

thickness is below 2 μm thick. For devices with a thickness close to 2 μm, significant charge carrier generation can happen in a highly defective area, which will negatively impact the device performance.

The observation that the doping of the CdTe film is not uniform could have significant implications with regards to cell performance, leading to an area for further optimization. The images shown in Figures 3 and 5 for Cu-anneal temperatures above 200 °C indicate that every grain will likely form its own diode and as every grain has a different carrier density, the strength of every diode will be quite different, with some grains being completely depleted. The devices seem to be forming *n-i-p* type devices near the front interface with intrinsic grains sandwiched between the *n*-type window layer and the *p*-type CdTe grains. The overall V_{oc} that is measured for the cell is therefore an averaged number over the total area of micro-diodes, with the weaker diodes bringing down the overall V_{oc}. As V_{oc} is an area in need of further improvement in CdTe-based solar cell devices, making the carrier density more uniform would lead to an understanding of whether the cell level V_{oc} is limited by the multitude of micro-diodes.

Concluding, in this paper we have demonstrated that SCM could be a valuable technique to better understand how CdTe-based PV devices work and what the role is of the various processing steps. The data obtained through SCM is in good agreement with the Hall measurement data. It also agrees with CV and DLCP data from the perspective of depletion depth, though the minimum carrier density obtained through CV and DLCP is not accurate for cases where the device is fully depleted.

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